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(54) Title: MULTISTANDARD DMT DSL TRANSMISSION SYSTEM

(57) Abstract

A digital subscriber line transmission system using QAM modulation on several equally spaced discrete tones, uses, at a high transmission rate, N = 4096/p tones spaced by 4.3125 kHz, where p is a power of 2.

MULTISTANDARD DMT DSL TRANSMISSION SYSTEM

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to discrete multitone
(DMT) based digital subscriber line (DSL) transmission systems
5 which allow high speed communication on twisted pair telephone
lines. The invention relates more specifically to a VDSL (Very
high speed DSL) system which can be used with several existing
or forthcoming standards.

Discussion of the Related Art

10 Figure 1 shows the spectrum of a signal transmitted
according to the ADSL and ADSL-Lite (asymmetric DSL) standards.
The ADSL standard uses quadrature amplitude modulation (QAM) on
each of 256 tones, the tones being equally spaced by
4.3125 kHz. Thus, as shown, the last tone has a frequency of
15 1.104 MHz. The ADSL-Lite standard only uses the first 128
tones.

As shown, a gap is left at the beginning of the
spectrum for "plain old telephone services" (POTS).

According to the ADSL standards, most of the tones
20 are used for reception, the few remaining tones being used for
transmission, hence the term "asymmetric DSL".

Current VDSL standardization proposals devise the use
of frequencies up to 11.04 MHz.

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Figure 2 shows the spectrum of a signal transmitted by a conventional VDSL time domain duplexing (TDD) system such as described in "VDSL Alliance SDMT VDSL Draft Standard Proposal", ETSI STC/TM6, 973T13R0, Lannion, France, September 29-October 3, 1997. This system uses 256 or 512 tones spaced, respectively, by 43 or 21.5 kHz. The last tone has a frequency of 11.04 MHz. All the tones are used for a same transmission direction at one time, the transmission direction being switched every other transmitted symbol.

Figure 3 shows the spectrum a signal transmitted by a conventional VDSL "Zipper" system as disclosed in patent application WO 97/06619. It uses 2048 tones spaced by 5.375 kHz, the last tone also having a frequency of 11.04 MHz. In this system, the tones used for transmission and for reception are chosen dynamically in order to cancel near-end crosstalk and near-end echoes.

Figure 4 very schematically shows a DSL transmission system at one end of a telephone line 10. An inverse fast Fourier transform (IFFT) circuit 12 receives N complex frequency domain coefficients, where N is the number of tones used by the system, i.e. 128 or 256 for the ADSL standards, 256 or 512 for the VDSL TDD system, and 2048 for the VDSL Zipper system. The IFFT circuit 12 generates, for each set of N coefficients, a time domain symbol. A symbol is thus the sum of N sinusoidal subcarriers of different frequencies corresponding respectively to the tones. The amplitude and phase of each subcarrier is determined by the corresponding frequency domain coefficient received by the IFFT circuit. The symbols are processed by a digital-to-analog converter 14 and a low-pass filter 16 and then transferred onto telephone line 10 through a hybrid line interface 18.

A cyclic prefix and a cyclic suffix are added to the symbol output by IFFT circuit 12 at 19. The cyclic prefixes are intended to eliminate intersymbol interference in the far-end receiver by providing a guard period during which the

propagation transients of the line may decay. The cyclic suffix is intended to cancel the effects of the sampling of discontinuities in near-end echoes.

Line interface 18 also receives incoming symbols from line 10. These incoming symbols are provided to a fast Fourier transform (FFT) circuit 20 through a low-pass filter 22, an analog-to-digital converter 24 and, if necessary, through a time domain equalizer 26.

The above mentioned cyclic prefix, in order to accomplish its role, has a minimum length independent of the symbol length. In DSL systems using a relatively low number of tones, such as ADSL and VDSL TDD, the transmitted symbols are short, whereby the minimum length of the cyclic prefix is so long that it causes a substantial efficiency loss in the data transmission. In this case, the cyclic prefix is chosen shorter than necessary and it is the role of the time domain equalizer 26 to complement the short cyclic prefixes in the elimination of the intersymbol interference.

In DSL systems using a large number of tones, such as in the VDSL Zipper system, the generated symbols are so long that the cyclic prefixes can be chosen at the necessary length without substantially affecting the efficiency of the transmission. In such systems, the time domain equalizer 26 is omitted.

Moreover, in a VDSL TDD system, since the IFFT circuit and FFT circuit are never used at the same time, it is a single circuit which performs both functions.

The IFFT and FFT circuits operate at least at twice the frequency of the last tone used by the system, i.e. 1.104 MHz for ADSL-Lite, 2.208 MHz for ADSL, and 22.08 MHz for the known VDSL systems.

It is clear that the ADSL standards and forthcoming VDSL standards differ in many ways (the number of used tones, the spacing between the tones, the operation frequency of the IFFT and FFT circuits...), which is likely to increase the

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number of types of modems capable of exploiting these standards.

SUMMARY OF THE INVENTION

An object of the invention is to provide a transmission system which will allow a single modem to exploit many DSL standards with a low complexity.

To achieve this and other objects, the invention provides a digital subscriber line transmission system using QAM modulation on several equally spaced discrete tones. At a high transmission rate, the system uses $N = 4096/p$ tones spaced by 4.3125 kHz, where p is a power of 2 ($p = 1, 2, 4, 8...$).

According to an embodiment of the invention, for transmitting at a low transmission rate according to an ADSL standard, only the first $n = 128$ or 256 tones are used with $p = 1$.

According to an embodiment of the invention, the system comprises, on the transmitter side, an inverse fast Fourier transform circuit having N frequency domain value inputs corresponding to said tones, among which only the first receive values corresponding to the n used tones, the remaining inputs being zeroed, a decimator providing one sample for every r samples output by the IFFT circuit, with $r = N/n$, and a digital-to-analog converter coupled between the decimator and a subscriber line.

According to an embodiment of the invention, the system comprises, on the receiver side, an analog-to-digital converter sampling the signal on the subscriber line at a frequency F/r, where F is the operating frequency of the IFFT circuit; an interpolator generating samples at frequency F from the samples provided by the analog-to-digital converter; and a fast Fourier transform circuit operating at frequency F and receiving the samples from the interpolator through a time domain equalizer. When all N tones are used, the time domain equalizer is bypassed.

According to an embodiment of the invention, the system is applicable to a standard using n first tones among the N tones, where n is a power of 2. It comprises, at a transmitter side, an IFFT circuit having a number of frequency domain inputs selectable at least among values N and n; and an operating frequency selectable at least among two values F and fn proportional, respectively, to the frequency of the last of the N tones at the high transmission rate, and to the last of the n tones.

According to an embodiment of the invention, the system comprises, at a receiver side, an FFT circuit having a number of frequency domain outputs selectable at least among values N and n; and an operating frequency selectable at least among values F and fn.

According to an embodiment of the invention, each of the IFFT and FFT circuits includes five radix-4 stages and a last radix-2 or radix-4 stage connected to operate in pipeline mode, the desired number of frequency domain inputs or outputs of the circuit being selected by bypassing an appropriate number of stages and by selecting the radix of the last stage.

The foregoing and other objects, features, aspects and advantages of the invention will become apparent from the following detailed description of embodiments, given by way of illustration and not of limitation with reference to the accompanying drawings.

Brief Description of the Drawings

Figure 1, previously described, shows a spectrum of signals transmitted according to the ADSL and ADSL-Lite standards;

figure 2, previously described, shows a spectrum of signals transmitted in a conventional VDSL TDD system;

figure 3, previously described, shows a spectrum of signals transmitted in a conventional VDSL "Zipper" system;

figure 4 partially and schematically shows a DSL transmission system;

figure 5 shows a spectrum of signals transmitted in an embodiment of a VDSL system according to the invention;

figure 6 partially and schematically shows an embodiment of a VDSL system according to the invention adaptable to the ADSL and ADSL-Lite standards;

figure 7 schematically shows an embodiment of an IFFT circuit used in a VDSL system according to the invention; and

figure 8 schematically shows an architecture of a universal DSL modem according to the invention, incorporating IFFT and FFT circuits according to figure 7.

Detailed Description

As illustrated by the spectrum of figure 5, an aspect of the invention is to extend the spectrum of an ADSL-Lite transmission in order to approach the maximum frequency used in conventional VDSL systems, i.e. 11.04 MHz. The number of tones should be a power of 2 to be compatible with IFFT and FFT circuits of conventional architecture. In the embodiment of figure 5, the invention uses 4096 tones spaced by 4.3125 kHz, whereby the last tone has a frequency of 17.664 MHz. By using 2048 tones, the last tone would have a frequency of 8.832 MHz, whereby the transmission rate is significantly reduced with respect to a system which uses tones up to the devised limit of 11.04 MHz.

An aspect of the invention is to note that such a system, using 4096 tones, is immediately usable with any standard using fewer tones at the same spacing, such as 128 or 256 (ADSL-Lite, ADSL).

To transmit data according to the ADSL or ADSL-Lite standards with the above solution, it is sufficient to just use the first 128 or 256 tones by providing corresponding coefficients to the first frequency domain inputs of the IFFT circuit, and by zeroing the remaining inputs. In reception mode, the FFT circuit will extract to its first 128 or 256 outputs the wanted coefficients, the remaining coefficients being zero.

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The only modification to bring to transmission system is to provide zero-padding and depadding circuitry for adapting the low rate of the effective digital data transmission to the fixed high operation speed of the IFFT and FFT circuits.

A drawback of such a system is however that it operates at the highest frequency, adapted to the highest transmission rate, whereas the effective data transmission rate may be much lower. This causes unnecessary extra power consumption of the analog front-end.

Figure 6 schematically shows an embodiment of a transmission system operating as described above and additionally provided with circuitry for reducing the power consumption. As an example, the system is intended to operate with 4096 tones and is used with the ADSL standard, which will only use 256 tones. As shown, only the first 256 inputs of IFFT circuit 12 and the 256 first outputs of FFT circuit 20 are used.

The IFFT and FFT circuits operate at 35.228 MHz, i.e. twice the frequency of the last of the 4096 tones. The IFFT circuit 12 thus generates samples at 35.228 MHz. These samples are provided to a decimator 30 which provides only every 16th sample to digital-to-analog converter 14. Digital-to-analog converter 14 then operates 16 times slower, i.e. at 2.208 MHz. Of course, the cut-off frequency of the low-pass filters 16 and 22 is adapted to the frequency of the digital-to-analog converter 14.

The analog-to-digital converter 24 is clocked to sample the received signal 16 times slower, i.e. at 2.208 MHz, and the samples are provided to an interpolator 32 which generates the missing samples to provide to FFT circuit 20 at 35.228 MHz.

With the above example, the power consumed by converters 14 and 24 is substantially reduced. This power consumption will be further reduced if the ADSL-Lite standard is used with the system.

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When the system is used at its highest transmission rate, the decimator 30 and the interpolator 32 are bypassed as shown by switches, and the analog-to-digital converter 24 is clocked at the same speed as the IFFT and FFT circuits, i.e. 5 35.228 MHz in the example.

A purpose of a second embodiment of the invention is to further reduce the power consumption when the system is used at lower transmission rates.

In order to reduce the power consumption, it would be 10 useful to also adapt the operating frequency of the IFFT and FFT circuits to the transmission rate effectively used, like the clock frequency of analog-to-digital converter 24 in figure 6. However, by changing the operating frequency of the IFFT and FFT circuits, the spacing of the tones is also changed, which 15 is not desired.

To avoid this, the invention provides IFFT and FFT circuits of variable size, which is equivalent to making variable the number of tones used by the system. Then, if the size of the IFFT an FFT circuits is reduced by a factor k, it 20 is sufficient to reduce the operating speed of the IFFT and FFT circuits by the same factor k for maintaining the spacing between the tones. In the example of figure 6, the number of tones will be reduced by a factor 16, whereby the IFFT and FFT circuits would operate 16 times slower, i.e. at 2.208 MHz, the 25 same frequency as analog-to-digital converter 24. Decimator 30 and interpolator 32 are unnecessary.

With this system, the total power consumption will be substantially proportional to the effective transmission rate used on the system.

30 In contrast to what could be expected, making variable the number of inputs or outputs of an IFFT or FFT circuit is particularly simple if the number remains a power of 2.

Figure 7 schematically illustrates an IFFT circuit of 35 a conventional pipeline type, modified according to the

invention for making the number of inputs variable. The IFFT circuit comprises 5 pipelined radix-4 stages 34 followed by a last stage 36 which may be switched between radix-2 and radix-4. The number of frequency domain inputs of the IFFT circuit is equal to the product of the radices of the stages. If the last stage is a radix-2, the IFFT circuit has 2048 inputs, whereas if the last stage is a radix-4, the IFFT circuit has 4096 inputs.

Preferably, the last stage 36 can be switched between a radix-4 or radix-2 operation mode by a switch signal R2. For this purpose, the stage is a full radix-4 and, for operating in radix-2 mode, suitable elements of the stage are bypassed.

Each stage receives and provides complex coefficients at the digital data transmission rate. Each complex coefficient, corresponding at the input of the first stage to one data word, has a real part and an imaginary part which are processed in two respective cycles, hence the operating frequency of the IFFT circuit is twice the data transmission rate. The operating frequency is set by a clock signal CK.

A radix-4 stage operates on 4 consecutive coefficients whereas a radix-2 stage only operates on 2 consecutive coefficients. Each coefficient provided by the last stage 36 is converted into two time domain samples by a complex to real converter 38.

The number of inputs corresponding to each stage is indicated in figure 7 at the bottom of the stages, a first value being the number of inputs when the last stage 36 is a radix-2, and a second value being the number a inputs when the last stage 36 is a radix-4. It thus clearly appears that the number of inputs of the IFFT circuit is selectable by bypassing one or several first stages of the circuit and by suitably selecting the radix of last stage 36.

For the ADSL-Lite standard, the first two stages 34 of the IFFT circuit are bypassed by a multiplexer 40, the radix

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of the last stage 36 is chosen equal to 2, and the clock CK has a frequency of 1.104 MHz.

For the ADSL standard, the first two stages 34 of the IFFT circuit are also bypassed by multiplexer 40, the radix of the last stage 36 is chosen equal to 4, and the frequency of clock CK is chosen equal to 2.208 MHz.

For a VDSL transmission with 2048 tones according to figure 5, none of the stages is bypassed, the radix of the last stage 36 is chosen equal to 2, and the frequency of clock CK is chosen equal to 17.664 MHz.

For a VDSL transmission with 4096 tones according to figure 5, none of the stages is bypassed, the radix of the last stage 36 is chosen equal to 2, and the frequency of clock CK is chosen equal to 35.328 MHz.

A VDSL-TDD transmission would be modified to use a maximum frequency of 17.664 or 35.328 MHz instead of 22 MHz.

For such a modified VDSL-TDD transmission with 512 tones, the first stage 34 is bypassed by a multiplexer 42, and the radix of last stage 36 is chosen equal to 2.

For a modified VDSL-TDD transmission with 256 tones, the two first stages 34 are bypassed by multiplexer 40, and the radix of last stage 36 is chosen equal to 4.

Finally, for the VDSL transmission of figure 5 with 4096 tones, none of the stages is bypassed, the radix of the last stage 36 is chosen equal to 4, and the frequency of clock CK is chosen equal to 35.328 MHz.

An FFT circuit with a selectable number of outputs is constructed in the same manner as the IFFT circuit of figure 7. The differences are that the first stage is preceded by a real to complex converter which provides the real and imaginary parts of each complex coefficient in reverse order. The initial order is re-established at the output of the last stage, which is not followed by a complex to real converter.

Further information on pipeline IFFT and FFT circuits can be found, for example, in "A Fast Single-Chip

Implementation of 8192 Points FFT", IEEE Journal of Solid State
Circuits, Vol. 30, N°3, March 1995, Pidet, Castelain, Senn,
Blanc.

It is devised, for VDSL-TDD and VDSL "Zipper" modems,
5   that the tones will be used in an initial phase to transmit
modem identification signatures. In other words, a transmitting
modem, before establishing a communication, will send a signal
conveying specific tones or "bare" carriers, chosen depending
on the standard among the possible tones. The receiving modem
10 will detect which tones are present in the signal and identify
the standard accordingly. For this purpose, the receiving modem
should be "tuned-in" on the transmitting modem from the start,
i.e. use at least the tones used by the transmitting modem.
Every 8th or every 4th tone of a VDSL Zipper modem is used by a
15 VDSL-TDD modem, whereby such an identification phase is
possible in both directions if only the 256 or 512 tones of the
VDSL-TDD system are used for the signatures.

If an ADSL modem should send signatures using
consecutive tones, a modem according to the invention should be
20 consistent with figure 5, i.e. use a tone spacing of 4.3125
kHz. However, since the signatures are not yet standardized, it
may be devised that an ADSL modem will send signatures using
only every p^{th} tone, where p is a power of 2. In this case, a
modem having variable size IFFT and FFT circuits according to
25 the invention may initially use a tone spacing of 4.3125 kHz
and 4096/p tones and be switched to use 128 or 256 tones with a
spacing of 4.3125 kHz upon identifying a remote ADSL modem.

Figure 8 partially and schematically shows an
architecture of a universal DSL modem incorporating IFFT and
30 FFT circuits 12' and 20' as described above. Elements shown in
previous figures are designated by same reference characters.
The IFFT circuit 12' is preceded by a mapper 50 which
associates complex coefficients to outgoing digital words.
Circuit 19 which adds cyclic prefixes and cyclic suffixes to
35 the symbols provided by IFFT circuit 12' also achieves pulse

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shaping. A windowing or frequency weighted averaging is achieved at 52 on the data provided by time domain equalizer 26 to FFT circuit 20'. The output of FFT circuit 20' is successively processed by a frequency domain equalizer 54, a radio frequency interference canceller 56 and a demapper 58 which achieves the inverse function of mapper 50.

The IFFT and FFT circuits 12' and 20' are controlled by a controller 60 as described above in relation with figure 7. Controller 60 also sets the sampling frequency of analog-to-digital converter 24 at the operating frequency of the IFFT and FFT circuits. Moreover, controller 60 bypasses the time domain equalizer 26 and the radio frequency interference canceller 26, as shown by switches, when the number of tones used by the system is equal to 2048 or 4096.

Elements of the architecture of figure 8 which are not further described are conventional and can be found in modems for existing standards, such as ADSL and ADSL-Lite (disclosed in Standard T1.413).

Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The invention is limited only as defined in the following claims and the equivalent thereto.

What is claimed is:

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CLAIMS

1. A digital subscriber line transmission system using QAM modulation on several equally spaced discrete tones, characterized in that, at a high transmission rate, the system uses $N = 4096/p$ tones spaced by 4.3125 kHz, where p is a power of 2 $(p = 1, 2, 4, 8, \ldots)$.

2. The system of claim 1, characterized in that, for transmitting at a low transmission rate according to an ADSL standard, only the first $n = 128$ or 256 tones are used with $p = 1$.

3. The system of claim 2, characterized in that it comprises, on the transmitter side:

- an inverse fast Fourier transform (IFFT) circuit (12) having N frequency domain value inputs corresponding to said tones, among which only the first receive values corresponding to the n used tones, the remaining inputs being zeroed,

- a decimator (30) providing one sample for every r samples output by the IFFT circuit, with $r = N/n$, and

- a digital-to-analog converter (14) coupled between the decimator and a subscriber line (10).

4. The system of claim 3, characterized in that it comprises, on the receiver side:

- an analog-to-digital converter (24) sampling the signal on the subscriber line at a frequency F/r, where F is the operating frequency of the IFFT circuit;

- an interpolator (32) generating samples at frequency F from the samples provided by the analog-to-digital converter; and

- a fast Fourier transform (FFT) circuit operating at frequency F and receiving the samples from the interpolator through a time domain equalizer (26);

wherein, when all N tones are used, the time domain equalizer is bypassed.

5. The system of claim 1, applicable to a standard using n first tones among the N tones, where n is a power of 2, comprising, at a transmitter side, an IFFT circuit (12') having:

5   - a number of frequency domain inputs selectable at least among values N and n; and

- an operating frequency selectable at least among two values F and fn proportional, respectively, to the frequency of the last of the N tones at the high transmission

10 rate, and to the last of the n tones.

6. The system of claim 5, characterized in that it comprises, at a receiver side, an FFT circuit (20') having:

- a number of frequency domain outputs selectable at least among values N and n; and

15   - an operating frequency selectable at least among values F and fn.

7. The system of claim 6, characterized in that each of the IFFT and FFT circuits includes five radix-4 stages (34) and a last radix-2 or radix-4 stage (36) connected to operate

20 in pipeline mode, the desired number of frequency domain inputs or outputs of the circuit being selected by bypassing an appropriate number of stages and by selecting the radix of the last stage.
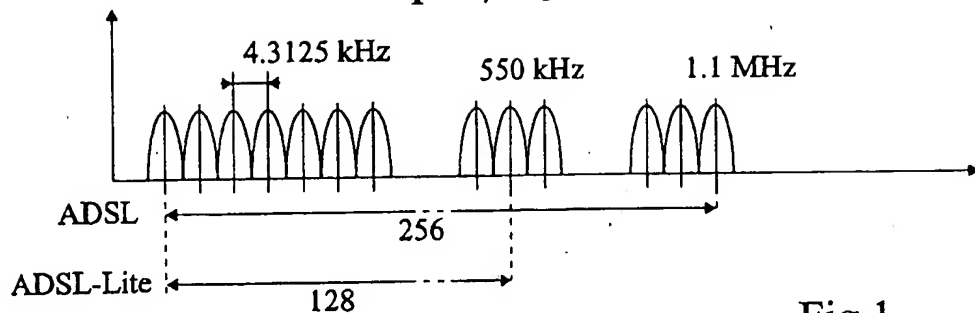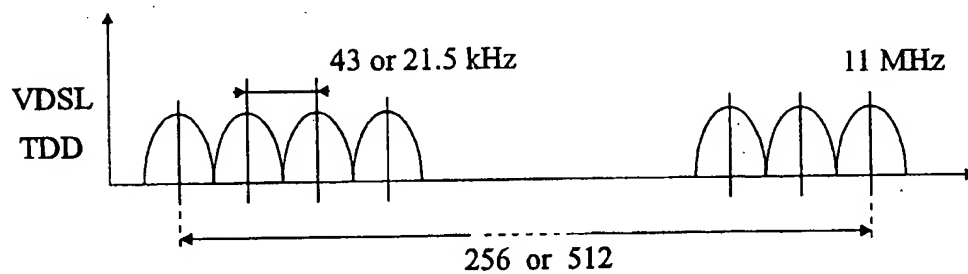
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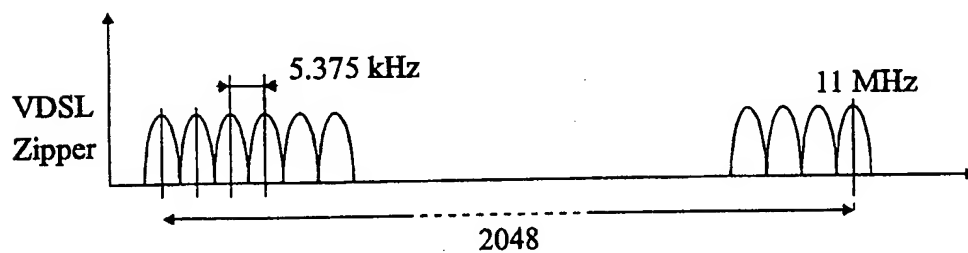Fig 1

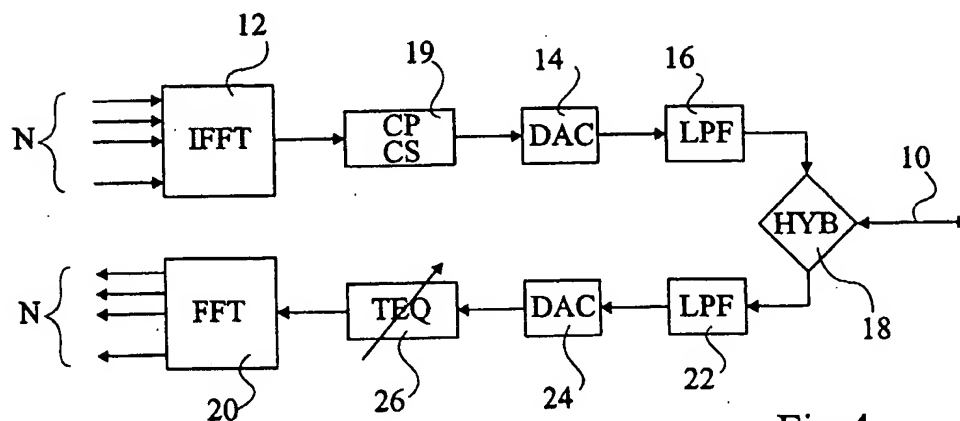
Fig 2

Fig 3

Fig 4
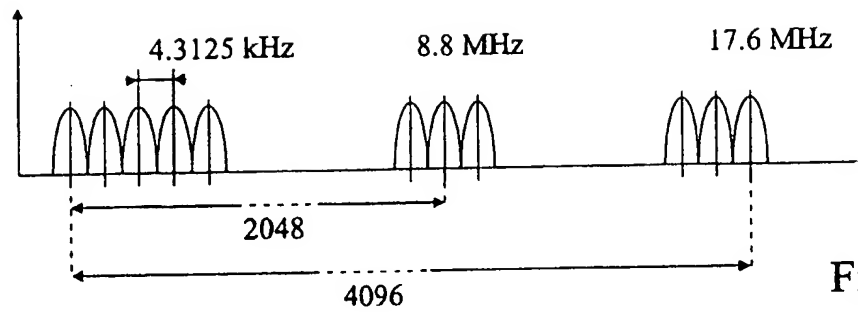
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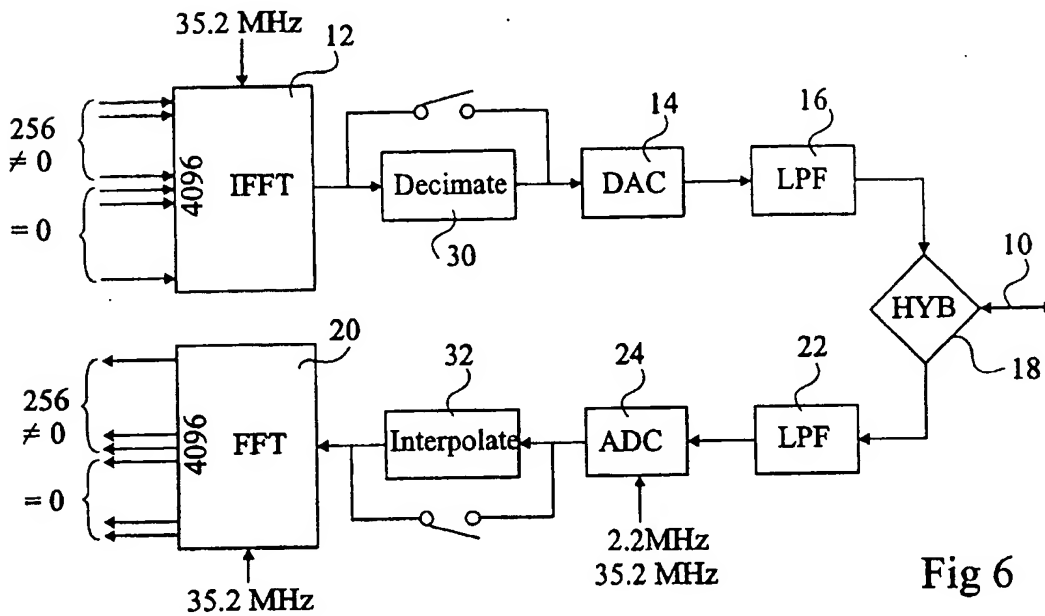
Fig 6
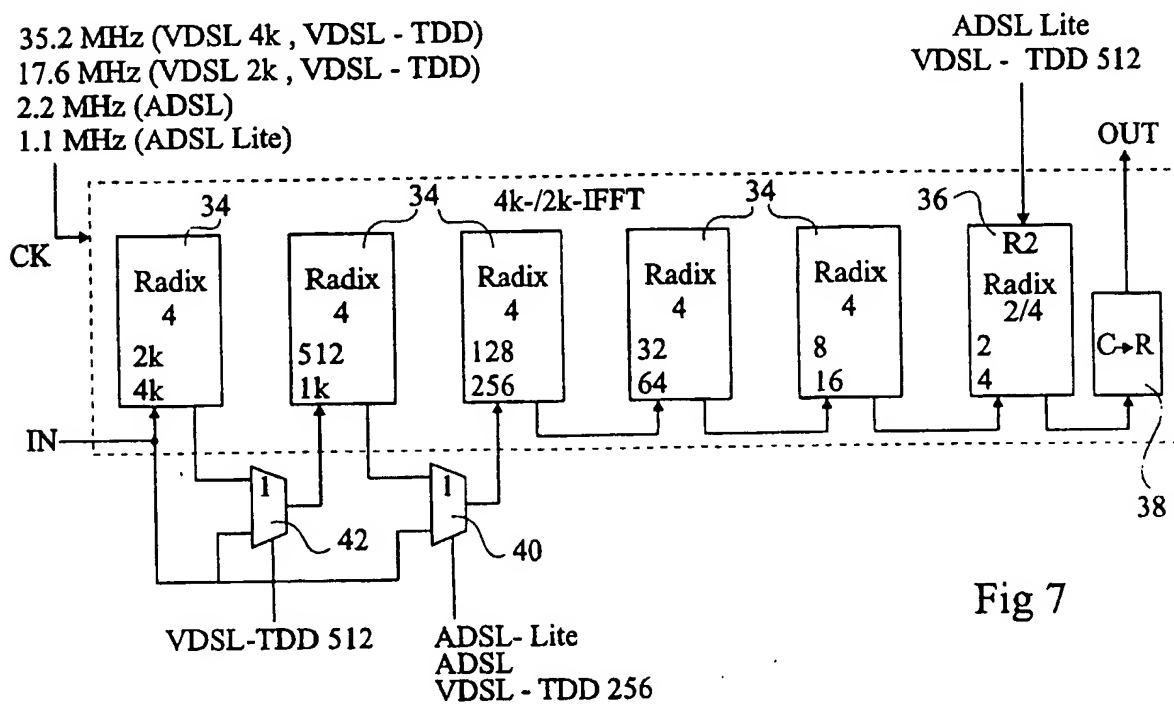
Fig 7
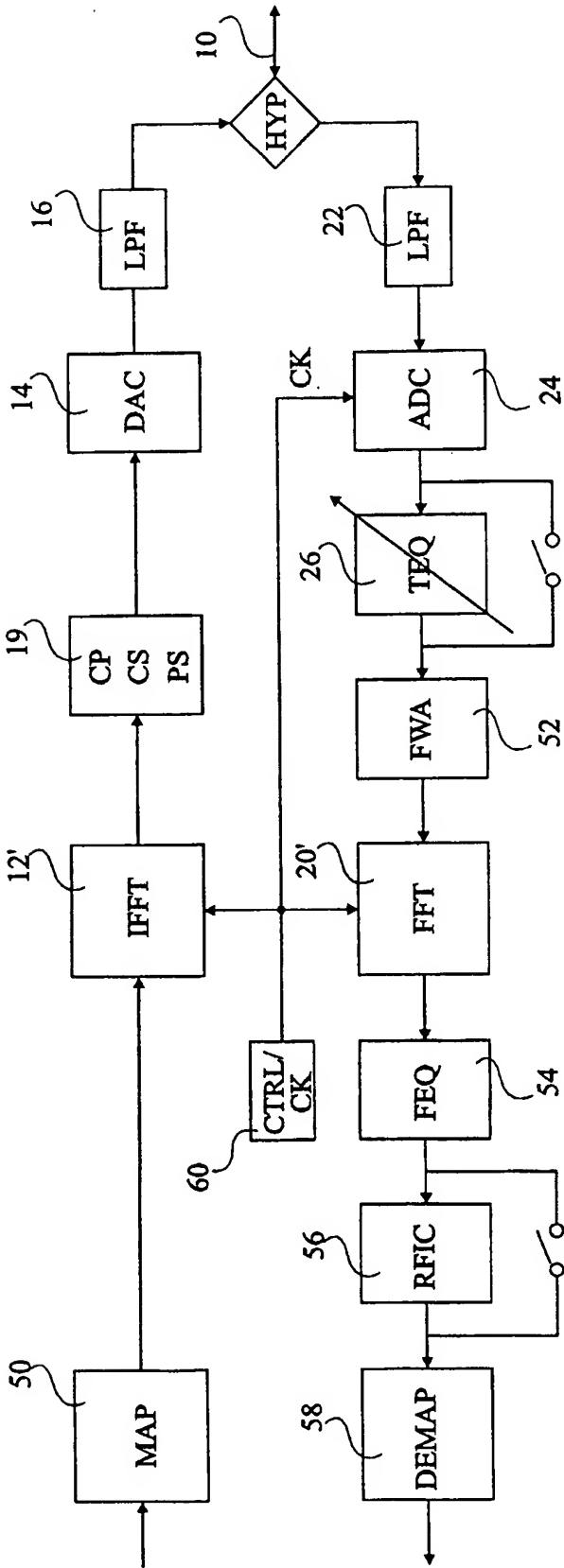
Fig 8

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7   H04L27/26

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7   H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 5 673 290 A (CIOFFI JOHN) 30 September 1997 (1997-09-30) abstract column 14, line 4 - line 49 column 7, line 66 -column 8, line 4 column 8, line 50 - line 55 figures 1,5 ___	1 2-4
A	EP 0 853 390 A (ANALOG DEVICES INC) 15 July 1998 (1998-07-15) page 6, line 27 -page 7, line 16 figure 4B ___ -/—	1-4

☒ Further documents are listed in the continuation of box C.   ☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 March 2000	27/03/2000

Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax (+31–70) 340–3016	Authorized officer Masche, C

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 795 984 A (MOTOROLA INC) 17 September 1997 (1997-09-17) abstract column 1, line 46 - line 55 column 6, line 31 - line 49 column 10, line 9 - line 21 figures 4,12	1-4

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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